Code No: **D0608**

**R09**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**M.Tech II - Semester Examinations, March/April 2011**
**CMOS ANALOG AND MIXED SIGNAL DESIGN**
**(DIGITAL SYSTEMS AND COMPUTER ELECTRONICS)**

**Time: 3hours**                                                                                        **Max. Marks: 60**

**Answer any five questions**
**All questions carry equal marks**
**- - -**

1) a) Explain how layout techniques improve the matching in MOSFET mirrors?
   b) Derive the expression for sensitivity of $I_0$ due to $V_{dd,}$ temperature coefficient TC of $I_0$.
   [12]

2) a) Draw the circuit of a Beta multiplier referred self biasing circuit and derive the expression for temperature coefficient.
   b) Using the Beta multiplier current reference, design a 10µA current source. Estimate the temperature coefficient and assume $V_{dd=}$ - $V_{ss=}$ 2.5v.  [12]

3) a) Explain two different types of gate drain connected load amplifiers.
   b) Draw the circuit of a shunt-shunt feedback amplifier and explain its working along with parameter calculations.  [12]

4) a) Explain the operation of a wide swing differential amplifier.
   b) Design a two stage CMOS OPAMP with the following specifications $A_0$=55000, GBW=1.2MHz, SR=2.5V/µsec.  [12]

5) a) Explain the design and analysis of a Tran conductance amplifier..
   b) Draw the circuit for cross coupled pair differential amplifier with active loads and derive the expression for $A_v$.  [12]

6) a) Explain dynamic comparator and dynamic biasing of current mirror circuits.
   b) Find the device dimensions of the input stage for a 2-stage comparator to meet the following specifications. Input common Mode Range is 1.5 v to 9v, $V_{dd}$=10v, $V_{ss=}$ 0v.
   [12]

7) a) Design a Zero temperature coefficient voltage Beat Multiplier reference at $300^0$k with $V_{ss=}$ 0v and $V_{dd}$=5v. Determine the sensitivity for changing $V_{dd}$ and Temperature T.
   b) Explain the basic building blocks of a switched capacitor circuit.  [12]

8) a) Design a bit current steering DAC using the generic current steering DAC. Assume that each current I is 5 mA and find the total output current for each input node.
   b) Explain different characteristics Parameters of ADC and DACS.  [12]

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